

REMARKS

The Office Action dated January 16, 2007 has been received and carefully noted. In response thereto, Applicant requests entry and consideration of the following remarks. No claims have been amended, no new claims have been added, and therefore, Applicants submit that no new matter has been introduced. Therefore, claims 1, 3, 5-11, 13-15, and 17-20 are pending and submitted for consideration herein.

As a preliminary matter, on page 2 of the Office Action the Examiner notes that a request for continued examination under 37 CFR §1.114 was filed in the present application after the final rejection. Applicants submit that this statement is erroneous and respectfully request correction of the record to reflect that Applicants filed a Pre-Appeal Brief Request for Review (along with a Notice of Appeal) on June 1, 2006, which was after the issuance of the Advisory Action dated May 18, 2006. Thereafter, on September 19, 2006, the Office issued a Notice of Panel Decision from Pre-Appeal Brief Review directing that prosecution in the present application be reopened and a new Office Action mailed. The current Office Action is the response to the Panel Decision. At no time have Applicants filed a request for continued examination under §1.114 in this application. Correction of the formal record is respectfully requested.

On page 3 of the Office Action, claims 1, 3, 5, 11, 13, 15, and 17-20 were rejected under 35 USC §102(b) as being anticipated by *Moslehi* (US Patent No. 6,124,198). The Office Action took the position that *Moslehi* teaches each and every element recited in the rejected claims. Applicants traverse the rejection and respectfully submit that each of claims 1, 3, 5, 11, 13, 15, and 17-20 recite subject matter that is not taught or disclosed by *Moslehi*.

Applicants' independent claim 1, from which each of claims 3-10 directly or indirectly depend, recites an integrated circuit package bond pad that includes an insulating layer, an electrode located over the insulating layer and having a plurality of discrete conductors separated by portions of a dielectric layer, wherein each of the plurality of discrete conductors has a first surface configured to be bonded to external circuitry and a second surface opposite the first surface. The bond pad is further recited as including a plurality of conductive members located in the insulating

layer, wherein ones of the plurality of conductive members contact the second surface of corresponding ones of the plurality of discrete conductors of the electrode.

Applicants' independent claim 11, from which claims 13 and 14 depend, recites a method of manufacturing an integrated circuit package bond pad. The method includes forming an insulating layer over a substrate, forming a plurality of conductive members in the insulating layer, and forming an electrode over the insulating layer. The electrode is recited as having a plurality of discrete conductors separated by portions of a dielectric layer, wherein each of the plurality of discrete conductors have a first surface configured to be bonded to external circuitry and a second surface opposite the first surface and contacting a corresponding one of the plurality of conductive members.

Applicants' independent claim 15, from which claims 17-20 depend, recites a method of manufacturing an electronic device. The method includes providing a substrate having a first bond pad located thereon, and providing an integrated circuit package having a second bond pad located thereon. The second bond pad includes an insulating layer and an electrode located over the insulating layer and having a plurality of discrete conductors separated by portions of a dielectric layer, wherein each of the plurality of discrete conductors has a first surface configured to be bonded to the first bond pad and a second surface opposite the first surface. The second bond pad further includes a plurality of conductive members located in the insulating layer, wherein ones of the plurality of conductive members contact the second surface of corresponding ones of the plurality of discrete conductors of the electrode. The method further includes forming a bond electrically coupling the first and second bond pads.

Therefore, each of Applicants' independent claims include the limitation of an electrode positioned over an insulating layer and having a plurality of discrete conductors separated by portions of a dielectric layer, wherein each of the plurality of discrete conductors has a first surface configured to be bonded to external circuitry and a second surface opposite the first surface.

Moslehi teaches a multi-level interconnect structure and fabrication process therefore. The interconnect structure includes a plurality of electrically conductive metallization levels, each of which has a plurality of electrically conductive interconnect lines. A plurality of electrically

conductive plugs make electrical connections between various metallization levels as well as between the metallization levels and the semiconductor devices fabricated on the same semiconductor substrate. The structure further includes a free-space medium occupying at least a substantial fraction of the electrically insulating regions within the multi-level interconnect structure surrounding the interconnect lines and plugs.

However, *Moslehi* does not teach or disclose a bond pad having an electrode positioned over an insulating layer and having a plurality of discrete conductors positioned therein, where the plurality of discrete conductors are separated by a dielectric layer. Rather, *Moslehi* teaches that the bond pad is a unitary conductive member (M6), as shown in Figure 8, that has an insulative dielectric layer formed over the top of the conductive member. The insulative dielectric layer is etched to generate “windows” to the conductive member (M6), as shown in Figures 9-12 of *Moslehi*. Thus, *Moslehi* teaches a conductive member that has a plurality of exposed bonding windows, which is clearly distinct from Applicants’ recited plurality of conductors separated by a dielectric material. The insulative material in *Moslehi* does not “separate” conductive members, as recited in each of Applicants’ claims 1, 11, and 15. Therefore, Applicants submit that *Moslehi* fails to teach or disclose each and every limitation recited in claims 1, 11, and 15. As such, reconsideration of the rejection of claims 1, 11, and 15, along with each claim depending therefrom, is respectfully requested.

On page 8 of the Office Action, claim 1, 3, 5, 11, 13, 15, and 17-20 were rejected under 35 USC §102(e) as being anticipated by *Seyyedy* (US Patent No. 7,126,200). The Office Action took the position that *Seyyedy* teaches each and every element recited in the rejected claims. Applicants traverse the rejection and respectfully submit that each of claims 1, 3, 5, 11, 13, 15, and 17-20 recite subject matter that is not taught or disclosed by *Seyyedy*.

Applicants’ independent claims 1, 11, and 15 are discussed above. *Seyyedy* teaches integrated circuits with contemporaneously formed array electrodes and logic interconnects. In Figure 3, *Seyyedy* teaches an insulating material 328 that contains an internal third level metal electrode M3 and a partially exposed fourth level metal electrode M4. However, *Seyyedy* does not teach or disclose a bond pad having an electrode positioned over an insulating layer and having a

plurality of discrete conductors positioned therein, where the plurality of discrete conductors are separated by a dielectric layer, as recited in each of claims 1, 11, and 15.

The Examiner has equated the third level metal electrode (M3) of *Seyyedy* with the “electrode located over the insulating layer” recited in Applicants’ claims. Rather, the electrodes (M4 and 343, as cited by the Examiner) are positioned *within* the insulative layer 328, as clearly shown in Figure 3, and not *over* the insulating layer. Further, element 343 of *Seyyedy*, which is cited by the Examiner as an electrode, is described in *Seyyedy* as an MRAM storage device. Applicants submit that an MRAM storage device is not equivalent to an electrode, and as such, the Examiner’s reliance upon the MRAM storage device to teach the electrode is submitted as being improper. Further still, each of Applicants’ independent claims recite that the electrode is positioned over an insulating layer, and that the conductors are separated by a dielectric layer. Thus, Applicants’ claims recite 2 distinct layers, which is also not taught or disclosed by *Seyyedy*’s single insulating layer 328. Finally, Applicants’ independent claims also recite that a plurality of conductive members located in the insulating layer *contact* the second surface of corresponding ones of the plurality of discrete conductors of the electrode. In *Seyyedy*, the electrodes M3 and M4 are separated by the MRAM storage device 343, and therefore, the device of *Seyyedy* cannot teach that a plurality of conductive members (M3) *contact* the second surface (the bottom of M4), as these two elements *are separated by the MRAM device 34* and do not “*contact*” each other, as expressly recited in each of Applicants’ independent claims.

For each of the above noted reasons, Applicants submit that *Seyyedy* clearly fails to teach or disclose each and every element recited in each of Applicants’ independent claims 1, 11, and 15. Therefore, reconsideration and withdrawal of the rejection of claims 1, 11, and 15, along with each claim depending therefrom, is respectfully requested.

Applicants note that with regard to the Examiner’s comments related to claims 9 and 18 and Applicants’ specification lacking disclosure of the critical nature of the claimed dimensions, Applicants respectfully point the Examiner to at least paragraphs [0003], [0004], [0005], and [0024]-[0026], where the size and shape of the features of the invention are described as providing a critical function (nature) of the invention that is both novel and unexpected.

On page 12 of the Office Action, claims 1, 3, 5, 11, 13, 15, and 17-20 were rejected under 35 USC §103(a) as being obvious over *Yu* (US Patent No. 6,703,286). The Office Action took the position that *Yu* teaches each and every element recited in the rejected claims. Applicants traverse the rejection and respectfully submit that each of claims 1, 3, 5, 11, 13, 15, and 17-20 recites subject matter that is not taught, shown, or otherwise suggested by the cited prior art.

Applicants' independent claims are presented above. *Yu* teaches forming a pattern of metal contact points 56 within the layer 52 of Intra Level Dielectric (ILD), as shown in Figure 3. A layer 56 of metal for the bond pad is deposited over the surface of the metal contact points 54 and over the surface of the layer 52 of ILD that separates the contact points 54, and then the individual contact pads 14 are formed from the metal layer 56, as shown in Figure 4. Then another dielectric layer 58 is deposited over the contact pads 14 and the layer of ILD 52. Then an opening 60 is formed into layer 58 to allow establishment of electrical contact between the (top surface of) the bond pad and the points of electrical contact provided in the surface of the substrate 70.

Yu does not teach, show, or suggest a bond pad having an electrode positioned over an insulating layer and having a plurality of discrete conductors positioned therein, where the plurality of discrete conductors are separated by a dielectric layer. *Yu* teaches a first conductor 54, but not the second conductor recited in each of Applicants' claims. Although the Office Action cites to element 60 of *Yu* as teaching the second conductor, Applicants submit that this conclusion is erroneous, as element 60 of *Yu* is expressly defined as an "opening" (*See*, column 6, lines 21-26) and is not in any way synonymous with a conductor. Therefore, Applicants submit that *Yu* fails to teach, show, or suggest each and every limitation recited in Applicants' claims 1, 11, and 15. As such, reconsideration and withdrawal of the rejection of claims 1, 11, and 15, along with each claim depending therefrom, is respectfully requested.

In conclusion, Applicants submit that each of claims 1, 3, 5-11, 13-15, and 17-20 recite subject matter that is not taught, shown, or otherwise suggested by the cited references, when taken alone or in combination. As such, reconsideration and withdrawal of the above noted rejections is respectfully submitted.

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Customer No. 42717

If for any reason the Examiner does not believe that the claims in the application are now in condition for allowance, the Examiner is respectfully requested to contact the undersigned attorney to arrange for a telephonic interview to expedite the disposition of this application.

Respectfully submitted,



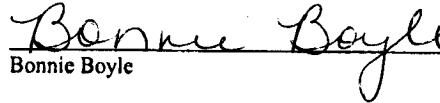
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